BATTERY-CONSERVING TRANSMISSION AND ENCODING METHOD FOR WIRELESS AD HOC NETWORKS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates generally to communication networks, and more specifically, to an apparatus and a method for communicating in a wireless network in a manner that conserves battery power.

Description of Related Art

[0002] Wireless networks having a number of battery-operated nodes distributed over a wide area are well known. In such networks, a receiver circuit in each node is either on at all times or is on at predefined time periods. When on, the receiver circuit may check for incoming messages. For example, in a Time Division Multiple Access (TDMA) network a receiver in a node may be on only during those time slots assigned to the node. In a second example, in Code Division Multiple Access (CDMA) Systems a receiver in a node is typically on all the time. In a third example, in Frequency Division Multiple Access Systems (FDMA), a receiver is typically kept on all the time or at least during the duration of a call. Having components of a receiver circuit powered on constantly or at predefined periods, whether or not incoming messages are arriving at the respective nodes can cause the batteries in the nodes to run down at a faster rate than batteries in nodes that use power in a more efficient manner.

[0003] Accordingly, power conserving nodes that increase an amount of time that a node may be able to operate without either replacing or recharging the node's battery are

desirable. Further, rechargeable batteries are generally able to be recharged a finite number of times before the battery will no longer accept a charge. Power conserving nodes would therefore make it possible to recharge node batteries less often, thus increasing the longevity of the rechargeable batteries.

SUMMARY OF THE INVENTION

[0004] Apparatuses and methods are provided for a wireless network that uses power efficiently.

[0005] One aspect of the invention is directed to a method for conserving power in a wireless ad hoc network. A device receives a burst via a wireless ad hoc network. The burst includes a preamble, a postamble and one or more blocks of data. The device is in either a low power state or a no power state when the preamble is first received. The device determines whether the preamble includes data indicating an ID of the receiving device. When the determining determines that the preamble includes the data indicating the ID of the device, the device derives from the preamble, information indicating a time and a duration for powering on one or more component of the device to receive one or more blocks of data included in the burst. The at least one component is powered on at a first time period based on the derived information in order to receive the data in the one or more blocks of data. The power remains on for a duration of time based on the derived information. The at least one component is powered off at a specific time period from a beginning of the first time period based on the derived information. The powering on and off is repeated for each of the one or more blocks of data in the burst. The received one or more blocks of data are then processed.

[0006] Another aspect consistent with the invention is directed to a method for encoding and transmitting a burst of data from a transmitter to a receiver using low or no power while waiting for reception of the data. A transmitter transmits a wake-up signal to a receiver and at least one block of data to the receiver. The wake-up signal provides structural information of an epoch, which includes the burst of data. The structural information is to be used by the receiver for reception of the burst of data.

[0007] Yet another aspect consistent with the invention is directed to a receiver configured to use low or no power. The receiver includes a correlator that is configured to use low or no power when waiting to receive data. A low noise amplifier is configured to receive and amplify analog signals from the correlator. An analog-to-digital converter is configured to convert the amplified signals from the low-noise amplifier to digital signals. Logic is configured to process the digital signals from the analog-to-digital converter. The correlator is configured such that when the correlator determines that the received data is received by an intended destination, the correlator generates a wake-up signal.

[0008] A transmitter is provided for transmitting a burst of data to a receiver that uses low or no power while waiting for reception of a burst of data. The transmitter includes a processor to process signals to be transmitted to the receiver. A digital-to-analog converter is configured to convert the signals from the processor from a digital form to an analog form. An up-converter is configured to convert the analog signals from a baseband to an RF band. A filter is configured to filter the RF band signal. An antenna is configured to transmit the RF band signal. The transmitter is configured to transmit a wake-up signal to the receiver. The wake-up signal includes structural information of an

epoch. The transmitter is further configured to transmit at least one block of data in a second epoch and is configured to remain in a powered off state until an existence of data to be transmitted.

[0009] In another aspect of the invention, a receiver is provided. The receiver is configured to use low or no power when waiting to receive a burst of data. The receiver includes means for correlating configured to use low or no power, means for amplifying received analog signals from the means for correlating, means for converting the amplified signals from the means for amplifying to digital signals, and means for processing the digital signals from the means for converting the amplified analog signals. The means for correlating includes means for generating a wake-up signal. When the means for correlating determines that the receiver is an intended destination of the received data, the means for generating the wake-up signal generates the wake-up signal.

[0010] In another aspect of the invention, a transmitter is provided for transmitting a burst of data to a receiver having low or no power. The transmitter includes means for processing signals including data to be transmitted to the receiver, means for converting the signals from the means for processing from a digital form to an analog form, means for up-converting the analog signals from a baseband to an RF band, means for filtering the RF band signal, means for retrieving location information of the receiver, and means for transmitting the RF band signal to the receiver. The transmitter is configured to transmit a wake-up signal to the receiver. The wake-up signal includes structural information of an epoch and is configured to transmit at least one block of data in a second epoch. The transmitter is configured to remain in a powered off state until an existence of the data to be transmitted. The means for transmitting further uses the

location information to transmit the wake-up signal to the receiver, such that the wake-up signal arrives at the receiver within a window of a time slot boundary at the receiver.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

[0012] Fig. 1 illustrates an exemplary wireless network including exemplary wireless nodes;

[0013] Fig. 2 is a block diagram of an exemplary node;

[0014] Fig. 3 is a block diagram of an exemplary receiver of the node in Fig. 2;

[0015] Fig. 4 is an exemplary transmitter of the node of Fig. 2;

[0016] Figs. 5A-5G are timing diagrams that illustrate timing, activation, and deactivation of components within an exemplary receiver;

[0017] Fig. 6 is a flowchart that illustrates processing in an exemplary transmitter; and

[0018] Figs. 7-8 are flowcharts that illustrate processing in an exemplary receiver.

DETAILED DESCRIPTION

[0019] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. The following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and equivalents.

[0020] The following U.S. Patents are incorporated herein by reference in their entirety: U.S. Patent No. 6,574,269, U.S. Patent No. 6,104,708 and U.S. Patent No. 6,590,889. U.S. Pat. No. 6,590,889 and U.S. Patent No. 6,104,708 disclose Direct Sequence Spread Spectrum (DSSS) multi-code-encoding methods and integrated TDMA-CDMA multiple access protocol techniques that permit a system that accommodates terminals and or links of different throughput capabilities to be in an integrated wireless digital network. U.S. Pat. No. 6,574,269 discloses methods that significantly simplify the implementation of a receiver in a wireless system that employs multi-code encoding. The methods taught by these patents may be used in implementations consistent with principles of the invention.

Hardware Overview

[0021] Fig. 1 illustrates an operating environment of an embodiment of the invention. A wireless network 100 is shown having four wireless nodes 102-1 through 102-4 (collectively, wireless nodes 102) that may communicate with one another. Wireless nodes 102 may send a message to another node in wireless network 100, where the other node may be a destination node or may be a relay node for relaying the message to yet one or more other nodes in order to eventually reach the destination node. Although Fig. 1 shows wireless network 100 as having four nodes 102, a wireless network may have fewer or more nodes.

[0022] Fig. 2 illustrates a detailed view of exemplary wireless node 102. Node 102 may have a transmitter 202 for transmitting messages, a receiver 204 for receiving messages, an antenna 207 and storage, for example, a memory 206, for storing, among

other things, one or more received messages and one or more messages to be transmitted, and a processor 208, such as a Digital Signal Processor (DSP) for controlling node 102.

[0023] Fig. 3 shows a detailed view of exemplary receiver 204 of node 102. Receiver 204 may include a correlator 304, an antenna 302, a low noise amplifier (LNA) 306, an analog-to-digital (A/D) converter 308, a receive FIFO buffer (RxFIFO) 310, a circuit activation controller (CAC), a processor 314, and a memory 316. Processor 314 may be a digital signal processor (DSP) or discrete logic, such as an application specific integrated circuit (ASIC) or a field programmable gate array (FPGA).

[0024] When not receiving signals intended for the node, node 102 may be in a sleeping state. That is, correlator 304 may be in a low or no power state while correlating received signals. Antenna 302 receives signals, for example, RF signals, which may have been transmitted by another node. Correlator 304 may receive the signals from antenna 302, determine whether the signals include a pseudo-random noise sequence (PRNS) that is associated with an ID or address of receiving node 102 and downconvert the signal from the received band to another band, for example, RF to baseband. Correlator 304 may determine whether a message is intended to be received by the receiving node by determining whether a PRNS in a preamble of the message, matches a predefined PRNS configured in correlator 304. When correlator 304 determines that the message is intended for receiving node 102, node 102 may be awakened from the sleeping state in stages, as will be explained later in more detail.

[0025] In some implementations, correlator 304 may be a Surface Acoustic Wave (SAW) correlator that uses little or no power when receiving messages and determining whether the received message was intended to be received by the node. An example of

such a correlator is available from Sandia National Laboratories of Livermore, California. The existence of such correlators makes possible low power transceivers, tags, locators, and no-power wake-up circuits.

[0026] Ultra low power Low Noise Amplifiers (LNAs) have recently been developed. One such LNA, for example, was developed by Sandia National Laboratories. Such a LNA, for example, LNA 306 may be used in embodiments of the invention and may amplify the signal from correlator 304. Analog-to-Digital converter (A/D) 308 may receive the amplified signal from LNA 306, convert the analog signal to a digital signal, and pass the converted digital signal to receive FIFO (RxFIFO) 310 buffer. Activation of LNA 306, A/D 308 and RxFIFO 310 is controlled by a Circuit Activation Controller (CAC) 312.

[0027] LNA 306, A/D 308, CAC 312, RxFIFO 310 and processor 314 are normally powered off when there are no incident bursts addressed to the receiving node or having the PRNS of the receiving node. CAC 312 may be activated by a wake-up pulse generated by correlator 304. The burst preamble may be encoded such that a pair of wake-up pulses are generated by correlator 304. The first wake-up pulse may activate CAC 312 and inform CAC 312 when to power on LNA 310, A/D 308 and RxFIFO buffer 310 while a burst is being received by correlator 304. LNA 306, A/D 308 and RxFIFO buffer 310 may not be powered on for the entire time in which the PRNS of the burst is being stored and correlated by correlator 304. The second wake-up pulse may inform CAC 312 when to power off LNA 306, A/D 308 and RxFIFO 310. Normally memory 316 and processor 314 are powered off or operate in a low power mode while the burst is being stored in RxFIFO buffer 310. The burst may be encoded such that an end of burst

pulse may be generated by correlator 304. The end of burst pulse may cause CAC 312 to power off LNA 306 and A/D 308 and instruct RxFIFO buffer 310 to wake up memory 316 and initiate transfer of the received samples stored in RxFIFO buffer 310. Normally data transfer from RxFIFO buffer 310 to the memory 316 is performed using direct-to-memory access (DMA) techniques that do not require processor intervention. A RxFIFO empty flag may cause processor 314 to become active. Processor 314 may then read the samples stored in memory 316, power off RxFIFO buffer 310 and process the data included with the burst. While the received data samples are being processed by processor 314 and while there is no incoming burst destined for the receiving node, LNA 306, A/D 308 and RxFIFO buffer 310 may be deactivated consuming little or no power. Processor 314 may remain active until the received message is queued for transmission to another node in the network or to a user interface port.

[0028] Fig. 4 illustrates exemplary transmitter 202 in detail. Receiver 204 may include a memory 401, a processor 402, a transmit FIFO buffer (TxFIFO) 403, a digital-to-analog converter (D/A) 404, an up-converter (U/C) 406, a power amplifier (PA) 408, a filter 410 and an antenna 412.

[0029] Processor 402 may be a processor, such as a DSP or discrete logic, such as an application specific integrated circuit (ASIC) or a field programmable gate array (FPGA). Processor 402 may prepare a message for transmission and send the resulting digital signals representing the message to TxFIFO 403 and digital-to-analog converter (D/A) 404. D/A 404 may convert the digital signals received from TxFIFO 403 to analog format and send the analog signals to U/C 406, which may convert the signals from one band, for example, baseband, to another band, for example, RF. The signals may then be

amplified by PA 408, filtered by filter 410 and transmitted to another node via antenna 412.

[0030] TxFIFO 403, D/A 404, U/C 406 and PA 408 are normally kept powered off while the TxFIFO 403 is empty to conserve power. TxFIFO 403 may be activated by processor 402 when there is a message to be transmitted. D/A 404, U/C 406 and PA 408 are activated and kept activated for the entire time the TxFIFO 403 is not empty.

[0031] Although Figs. 3 and 4 show the transmitter and receiver each having a dedicated antenna, processor and memory, a single processor, memory and antenna may be shared by the transmitter and receiver in some implementations.

Concept of Operations

[0032] The following explains operational aspects of some implementations in which components of a receiver are powered on and off to receive and process signals and are otherwise in a powered off or a low power state. The operational aspects are explained with reference to timing diagrams of Figs. 5A-5G and flowcharts of Figs. 6 and 7.

[0033] Figs. 5A-5F are exemplary timing diagrams that help illustrate operational aspects of implementations consistent with principles of the invention. The timing diagrams will be explained with exemplary nodes that use Code Division Multiple Access (CDMA) and a Direct-Sequence Spread Spectrum (DSSS) technique to modulate and Multi-Code (MC) encode signals including the message.

[0034] In one implementation, all nodes in the network have a common notion of time intervals or time slots in absolute terms. That is, all nodes in the network may be synchronized. Synchronizing nodes in a network is well known. Some ways that this

may be accomplished include utilizing GPS information or atomic clocks. Fig. 5B illustrates synchronized atomic clock time slots in an exemplary implementation.

[0035] Figs. 5C-5G are timing charts showing the time of a transmission of an exemplary message having a preamble 502, a postamble 504, and multiple blocks of data 506. Each receiver may have a predefined ID, such as a MAC ID, defined at manufacturing time. The preamble, data blocks and postamble may include one or more DSSS shift-orthogonal-codes, where each shift-orthogonal-code is a cyclic-shift version of a selected base PRNS, having encoded therein a MAC ID or other indication of an intended destination node. Each shift-orthogonal-code when correlated with or passed through a filter that is matched to the selected base PRNS produces at its output a pulse that reproduces an impulse response of an underlying transmission channel and a shift-delay of each shift-orthogonal-code with respect to the base PRNS. Preamble 502 may include two high-gain shift-orthogonal-codes with easily detectable wake-up pulses at the output of the matched filter or correlator. The two shift-orthogonal codes of the preamble are a distance of M+K codes apart, where M is the number of modulated-data symbols or bits transmitted per data block 506 and K is a number of chip times required for M bits to be flushed from a correlator, such as, for example, correlator 304. The first and second shift-orthogonal-codes are cyclically padded at the end and at the beginning respectively, each with at least M+K-1 chips of cyclic padding to enforce the orthogonality of the signals being received and the exact reproduction of the impulse response of the underlying transmission channel for each of the cyclic-shift-codes received. A length of a Finite Impulse Response (FIR) determines a size of K.

[0036] In some implementations, each node may store information concerning locations of other nodes. The relative location information, for example, node xyz coordinates, can be used to determine signal attenuation as the signal propagates from the transmitter to the receiver and the Signal to Noise Ratio (SNR) of the received signal at the output of the correlator, for example, correlator 304. Alternatively, the SNR can be estimated by comparing, for example, the relative peak power of the preamble wake-up pulses with the average power of the signal in between such pulses. The SNR, together with a message Quality of Service (QoS) information, for example Bit Error Rate (BER), determines the number of modulated-data-symbols per data block and the maximum allowed delay determines the modulation technique and the number of bits per modulated-data-symbol. Modulation techniques for multiple-bits per modulated-data-symbol are very well known, such as M-ary Phase-Shift-Keying (PSK), M-ary Pulse Amplitude Modulation (PAM) and M-ary Quadrature Amplitude Modulation (QAM), with $M=2^b$, where "b" is a number of bits per modulated-data-symbol.

[0037] The relative location information may be used to determine the propagation delay and a time to transmit a message to a specific node such that the message arrives at the specific node within a small time window. Techniques for obtaining signal propagation delays are well known, such as distance calculations using node coordinates, for example, using GPS, or direct propagation delay measurements using spread spectrum techniques with maximal-length pseudo noise sequences (m-sequences) or spread spectrum codes with correlation properties similar to the shift-orthogonal-codes included therein.

[0038] When receiver 204 receives the pseudo-random noise (PN) sequence codes having the high-gain wake-up pulse, the received codes may be matched by correlator

304 to detect the first wake-up pulse. The processing gain at the output of the correlator may be 10 Log_{10} L/M, where L is a length of the shift-orthogonal-code, excluding the cyclic padding, and M is the number of shift-orthogonal-codes per block (M=2 for the preamble 502 and postamble 504 and M=L-K for the transmitted data blocks 506).

[0039] In some implementations, counters may be activated to count the amount of time between the first and second wake up pulses from the preamble. The determined amount of time, M+K, may be used to determine when to power on and off A/D 308, LNA 306 and RxFIFO 310. In some implementations, the wake-up pulses may not be permitted to activate the counters unless collision free reception of the preamble is determined with high probability. That is, the first wake-up pulse, matched to the correlator 304, must be detected within a narrow time window, for example, two chip times, of a time-slot boundary. The amplitude of the wake-up pulses and/or the power of the signal between pulses and/or in other points of the time-slot may be used to determine whether a collision occurred, as well as to estimate signal-to-noise ratio. In some implementations the relative positions of the detected pulses with respect to the time-slot boundaries may be measured and, after the relative positions are sent back to the transmitter, the transmitter may correct the estimated propagation delay. In some implementations the form and power of the signal between pulses and/or in other points of the time-slot may be used to measure the multipath, for example, from signal reflections, and may be used to further improve the SNR of the pulses received in the data blocks. Techniques to increase the SNR using the multipath-reflected signal energy are well known and include techniques such as RAKE processing at the receiver, for example, to constructively and/or coherently combine the signal energies from two or more multipaths, and/or signal

precoding by the transmitter, for example, to encode the transmitted signals such that the direct-path and one or more reflected signals arrive time-synchronized at the intended receiver node.

[0040] Blocks of data 506 or sub-bursts may each include a portion of the message. Each block 506 may include consecutive shift-orthogonal-codes of length L and M+K cyclic padding chips, where a chip is a smallest element of data in an encoded signal. The splitting of the cyclic padding chips at the start and at the end of each shift-orthogonal-code vary by one for each consecutive code, starting with the first shift-orthogonal-code will all M+K cyclic padding chips at the end. Each chip may be a binary number, an integer-valued number, a real-valued number, or a complex-valued number. Each modulated data symbol may convey information of one or more bits. M of the shift-orthogonal-codes may be transmitted simultaneously (superimposed) in each block. Each shift-orthogonal-code may be encoded by being multiplied, chip by chip, by a bit or a modulated-data-symbol. With multi-code encoding and binary modulation such as Binary-Phase Shift Keying (BPSK), the message is divided in blocks of bits with as many bits per block as the number of shift-orthogonal codes being transmitted simultaneously, and distinct bits of each block are encoded using different shift-orthogonal-codes, each shift-orthogonal-code being a different cyclic-shift of a base PRNS. With multi-code encoding and multi-bit modulation such as M-ary QAM with $b=\log_2 M$ bits per symbol, the message is divided in blocks of bits with as many bits per block as the number of bits "b" per modulated-data-symbol multiplied by the number of shift-orthogonal-codes being transmitted simultaneously, and distinct modulated-data-symbols of each block are encoded using different shift-orthogonal-codes. As illustrated in the exemplary charts

of Figs. 5A and 5C, each of the blocks of data are transmitted within a time period of L+K+M. Each of these L+K+M time periods having a block of data to transmit may be referred to as a time-slot or an epoch. Postamble 504 includes two shift-orthogonal-codes cyclically shifted K bits from each other.

[0041] Figs. 5D-5E help to explain the waking up of components of a receiver in stages in an exemplary implementation. Before the correlator determines that node 102 is an intended destination of a message, power in the node may be either low or off. At the point 508, after correlator 304 determines that the message is intended for the receiving node 102, the first wake-up pulse is detected and a counter may be started. At the point 510, the second wake-up pulse is detected and the counter stopped. Thus, in this example, the counter measures a time corresponding to M+K chip times. If a collision is detected, the receipt of the message is aborted. The required counters as well the circuits and/or logic required to detect collisions may be included in CAC 312.

[0042] At the point 512, after receipt of an L length code in a first epoch of the message, LNA 306,A/D 308 and RxFIFO 310 may be powered on. A/D 308 may be powered on for a period of M+K chips and then powered off at the point 514. This period is long enough to convert M chip times worth of data from analog to digital format and to allow any remaining data to be flushed from correlator 304. RxFIFO 310 and A/D 308 power on and off times may be delayed with respect to each other to accommodate internal delays in the A/D 308 circuitry.

[0043] At the point 516, after receipt of an L length code in a second epoch of the message, LNA 306, A/D 308 and RxFIFO 310 are powered on for a period of M+K chip times and then powered off at 518.

[0044] At the point 520, after receipt of an L length code in a third epoch of the message, LNA 306, A/D 308 and RxFIFO 310 are powered on for a period of M+K chip times and then powered off at 522.

[0045] At the point 524, correlator 304 detects an end of burst pulse corresponding to the first shift-orthogonal code in the postamble. At the point 526, a time period of K chip times after reception of the first shift-orthogonal-code, correlator 304 detects a second pulse corresponding to the second shift-orthogonal-code in the postamble indicating that the burst reception has completed and that the received burst stored in the RxFIFO 310 is ready to be transferred to memory 316. Data transfer from RxFIFO 310 to memory 316 may be implemented while a processor 314, such as a DSP, is powered off or operating in a low power mode using well known direct-to-memory transfer techniques, for example, using Direct-Memory Access (DMA) devices. After the data transfer to memory 316 has completed, processor 314 may be powered on to process the complete message and may then be powered off.

[0046] Fig. 5F illustrates the sampling of data received during sub-bursts 506. Each of the K+M chip times worth of modulated-data-symbols of each sub-burst may be sampled by A/D 308 at least once per chip time and typically four times over the K+M chip time interval. It is well known that the wider the bandwidth of filter 410, the faster A/D 308 has to operate. Consequently, the faster A/D 308 operates, the more power A/D 308 consumes. In some implementations, the bandwidth of filter 410 may be optimized such that A/D 308 may operate at a rate of one sample per chip time, thereby minimizing power consumed by A/D 308.

[0047] Fig. 5G illustrates points at which LNA 306 and A/D 308 are powered on and off in an implementation consistent with the principles of the invention. As can be observed, LNA 306 and A/D 308 are powered on only for a time period having a duration of M+K chip times beginning immediately after reception of a first code within preamble 502 and within each block of data 506.

Transmitter Processing

[0048] Fig. 6 is a flowchart illustrating exemplary processing for the transmission of messages from one of exemplary nodes 102. Transmitter 202 may sleep until a packet is queued for transmission (act 600). When a packet is queued for transmission, node 102 may determine whether the destination node can be reached directly or whether another node must be used to relay the message to be transmitted to the destination node (act 602). Node 102 obtains the ID or address of the next node (act 604) and link budget and synchronization information (act 606). Based on the link budget and on message QoS parameters, such as BER and maximum delay, node 102 may determine a number or bits per modulated-data-symbol and a number of shift-orthogonal-codes to use when transmitting epochs 506 (act 608). The message is then transmitted to a receiving node (act 610) in the form shown in Fig. 5C while powering on-and-off the transmitter modules 402 through 412 as required, as previously discussed. If no other packets are queued for transmission, node 102 goes to sleep until another packet is queued for transmission (act 600).

Receiver Processing

Fig. 7 is a flowchart illustrating exemplary processing for the reception of messages in one of nodes 102. Receiver 204 sleeps until wake-up pulses are detected (act 702). The

wake-up pulses may be generated by correlator 304 when correlator 304 detects an ID match that matches the correlator PRNS while processing a preamble. CAC 312 may determine whether the first of two wake-up pulses occurs within a narrow window close to a beginning of a time slot, for example, within two chips times, and whether the detection can be performed free of collision and/or within acceptable levels of interference (act 704). If not, the receiver goes to sleep (act 702). If a collision is detected at this point (act 706), the reception of the message may be aborted (act 710) and the receiver goes to sleep (act 702). Otherwise, more circuits are awakened (act 708) as previously described with respect to Figs. 5E and 5G. A data block is received and stored in RxFIFO 310 (act 712), as previously described with respect to Figs. 5E and 5G (i.e., LNA 306, A/D 308, RxFIFO 310 and processor 314 are powered on and off as described previously). After receiving each block, a check may be made to determine whether a collision occurred and whether the data block was received within acceptable levels of interference (act 714). If a collision was detected or the interference was not within acceptable levels, the reception may be aborted (act 710) and the receiver goes to sleep (act 702). Otherwise, CAC 312 may determine whether a postamble was detected (act 802). If no postamble was detected, then receiver 204 may wait for the next data block (act 803). If the postamble was detected, then memory 316 may be powered on and contents of RxFIFO 310 may be moved to memory 316 (act 804). CAC 312 may, upon detection of an empty RxFIFO 310, activate processor 314 (act 806). Processor 314 may then process the received message in memory (act 810), Receiver 204 may then sleep until wake-up pulses are detected (act 702).

Conclusion

[0049] Methods and systems consistent with the principles of the invention may provide a power-conserving method for transmitting and receiving data in a wireless network.

[0050] The foregoing description of preferred embodiments of the invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations will be apparent to those skilled in the art in light of the above teachings or may be acquired from practice of the invention.

[0051] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used. The scope of the invention is defined by the claims and their equivalents.